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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,918	07/09/2001	Ken Fernald	CYGL-24,692	7118

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EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,918	FERNALD, KEN	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There does not appear to be support for the lower logical address portion not having lock bits. Figure 11 clearly shows both portions (1102 & 1104) of memory 1106 containing lock bits. If the variable location is indicated by item 1118 in figure 11, then there still appears to be lock bit 1108 in portions lower than that. Also, there does not appear to be support for portions with lower logical memory addresses being erased before portions with higher logical addresses. In fact, no sequence of erasure can be found by the Examiner. The Examiner asks the Applicant to provide support for these limitations.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 1 and 8 recite the limitation "on one of the logical portions thereof" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

6. Claims 8-14 are objected to because of the following informalities: Claims 8-14 appear to be identical to claims 1-7. Appropriate correction is required. .

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Zimmer et al. (US Patent # 6,633,964).

9. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Sharma et al. (US Patent # 6,636,906).

10. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Wolrich et al. (US Patent # 6,681,300).

11. With respect to claims 1 and 8, Hotley discloses:

storing in a location in memory on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space and determinative as to the access thereof for a predetermined memory access operation thereon, as shown by the lock bits (item 54a) located in a separate logical column, for each row (54b) of the memory array in figure 4;

detecting a request for access to a desired location in the memory space for operating thereon, as shown in figure 6b;

comparing the requested memory access operation with the associated lock bit in the associated logical portion and determining if access is allowed for the requested memory access operation, and performing the requested memory access operation if allowed, as shown by protection determination and ensuing execution starting in step 626 in figure 6b;

there being at least two different memory access operations, as taught in column 9, lines 2-6.

12. With respect to claims 2 and 9, Hotley discloses the operation being a read of an addressable location, as recited in column 9, lines 2-6.

13. With respect to claims 3 and 10, Hotley discloses the operation being a write of an addressable location, as recited in column 9, lines 2-6.

14. With respect to claims 4 and 11, Hotley discloses the operation being an erase of the associated logical portion of an addressable location therein, by teaching in column 9, line 25, of a block erase operation.

15. With respect to claims 5 and 12, Hotley discloses:

storing the plurality of lock bits in a variable location in the memory and storing the location of the lock bits in a known location in the memory, as shown by one lock bit being stored for each row of memory in figure 4;

in the step of comparing, the location of the lock bits is first read from the known location in memory and then this read location is utilized to read the lock bits are read from memory, by teaching in column 13, lines 24-35, that each step instruction causes the middle address bits stored in the address latch counter 30-3 to be incremented by one for readout of the next lock bit location LMB1, then contents of the location LMB1 is compared with the key bit presented by ACP 10 which is the first key bit of the sequence to be compared.

16. With respect to claims 6 and 13, Hotley discloses the predetermined operation being an erase of the lock bits, by teaching in column 11, lines 10-15, that when a block is erased, all of its data including the lock bits stored in the lock storage area are set to ONEs.

17. With respect to claims 7 and 14, Hotley discloses the operation of erasing the lock bits requires that each of the lower logical portions with lower logical portions of the memory space relative to the variable location and not containing lock bits to be erased before the top most portion with higher logical addresses that contains the lock bits, by teaching in column 14, lines 15-20, of an erase being performed on the block designated by the most significant bits contained in the counter.

18. With respect to claims 1 and 8, Hotley teaches all other limitations, as discussed above, but fails to specifically disclose using the lock bits to determine if the requested predetermined type of access is allowed.

19. Zimmer et al. teach in figure 2B and column 4, lines 40+, of both a read lock bit and a write lock bit which would lock access to the memory block for either a read access type or a write access type.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Zimmer *et al.* before him at the time the invention was made, to modify the lock bits taught by Hotley, to include separate lock bits for both read and write access types, as with the lock bits of Zimmer *et al.*, in order to prevent undesired memory accesses and possible data loss/corruption, as taught by Zimmer *et al.*.

21. Sharma et al. teach in figure 3, of a read lock bit which would lock access to the memory block from a predetermined access type, wherein the access type locked is a read.

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Sharma *et al.* before him at the time the invention was made, to modify the lock bits taught by Hotley, to include a read lock bit, as with the lock bits of Sharma *et al.*, in order to prevent undesired read type memory accesses and possible data loss/corruption, as taught by Sharma *et al.*.

23. Wolrich et al. teach in figure 3, of a read lock bit which would lock access to the memory block from a predetermined access type, wherein the access type locked is a read.

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Wolrich *et al.* before him at the time the invention was made, to modify the lock bits

taught by Hotley, to include a read lock bit, as with the lock bits of Wolrich *et al.*, in order to prevent undesired read type memory accesses and possible data loss/corruption, as taught by Wolrich *et al.*.

Response to Amendment

25. In response to the amendment filed 5/2/05: claims 1-7 have been amended, and new claims 8-14 have been added.

Response to Arguments

26. Applicant's arguments filed 5/2/05 have been fully considered but they are not persuasive.

27. With respect to the independent claims, the Applicant alleges that the lock bits in Hotley are not contained in a separate logical portion of the memory space. Figure 4 of Hotley though shows the lock bits in a separate logical column from the rest of the data bits.

28. With respect to the independent claims, the Applicant alleges that the lock bits in Zimmer, Sharma, and Wolrich, are not contained in a separate logical portion of the memory space, but are in separate memory device altogether. The claims, though, do not limit the memory space to a single physical medium. Only a separate logical portion of the memory space is claimed. As such, a separate physical memory medium logically associated with the data array would read upon the claim language.

Conclusion

29. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar access limiting systems.

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
Primary Examiner
Art Unit 2186